TOSHIBA

TC531000CP-12/15
TC531000CF-12/15

SILICON STACKED GATE CMOS

131,072 WORD x 8 BIT CMOS MASK ROM

Description

The TC531000CP/CF is a 1,048,576 bit read only memory organized as 131,072 words by 8 bits. A low bit cost makes it suitable for use as program memory for microprocessors or for fixed data storage such as a character generator. The TC531000CP/CF uses CMOS technology and is suitable for low power applications where battery operation is required.

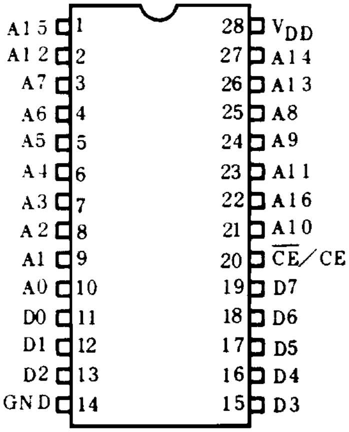
The TC531000CP/CF has a programmable chip enable input ($\overline{CE}$/CE) for device selection. This ROM is available in two speed versions. The TC531000CP/CF-12 is the 120ns version while the TC531000CP/CF-15 is the 150ns version.

Features

TC531000CP/CF	-12	-15
Access Time (max.)	120ns	150ns
Operating Current (max.)	40mA	35mA
Standby Current (max.)	20μA	20μA

- Single 5V power supply
- Inputs and outputs TTL compatible
- Three state outputs
- Fully static operation
- Programmable chip enable
- Package
  - TC531000CP : DIP28-P-600
  - TC531000CF : SOP28-P-450

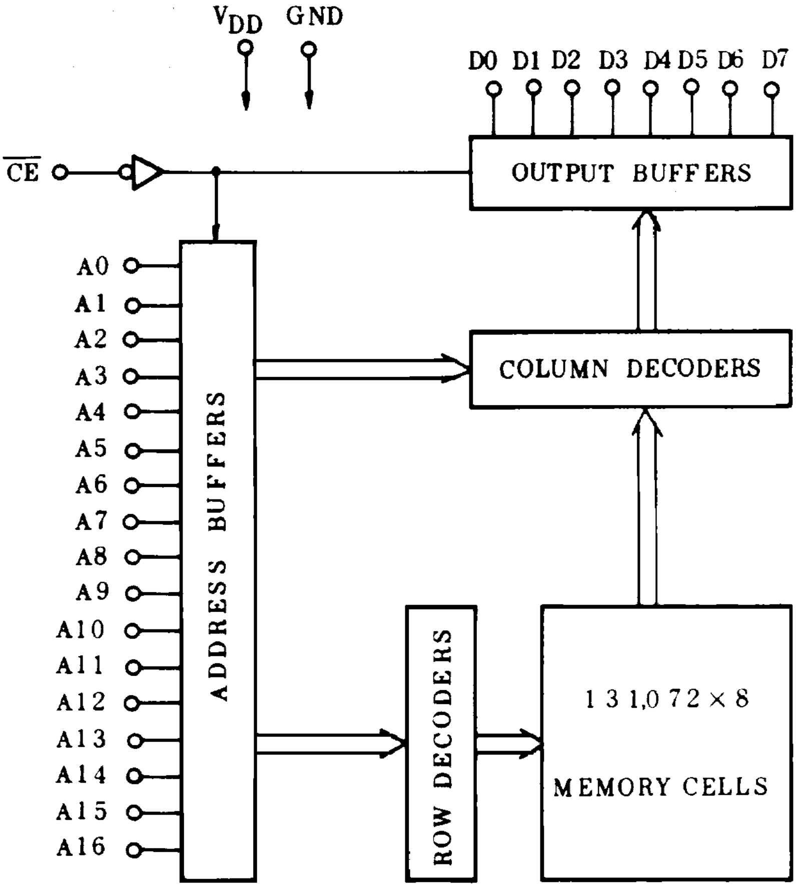
Pin Connection (Top View)



Pin Names

A0 ~ A16	Address Inputs
D0 ~ D7	Data Outputs
$\overline{CE}$/CE	Chip Enable Input
V_{DD}	Power Supply Voltage (+5V)
GND	Ground

Block Diagram



Operating Mode

MODE	$\overline{CE}$ (CE)	A0 ~ 16	OUTPUTS	POWER
Read	L (H)	Valid	Data Out	Operating
Standby	H (L)	*	High-Z	Standby

H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-0.5 ~ V_{DD}	
V_{OUT}	Output Voltage	0 ~ V_{DD}	
P_D	Power Dissipation	1.0/0.6*	W
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-40 ~ 70	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

* SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3	–	0.8	

DC Characteristics (Ta = -40 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}		–	±5.0	
I_{OH}	Output High Current	V_{OH} = 2.4V		-1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		3.2	–	
I_{DDS1}	Standby Current	CE = 0.8V($\overline{CE}$ = 2.2V)		–	2	
I_{DDS2}	Standby Current	CE = 0.2V ($\overline{CE}$ = V_{DD} - 0.2V)		–	20	μA
I_{DDO1}	Operating Current	V_{IN} = V_{IH}/V_{IL} I_{OUT} = 0mA	t_{cycle} = 120ns	–	50	mA
			t_{cycle} = 150ns	–	45	
I_{DDO2}		V_{IN} = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle} = 120ns	–	40	
			t_{cycle} = 150ns	–	35	

AC Characteristics (Ta = -40 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	-12		-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{CYC}	Cycle Time	120	–	150	–	ns
t_{ACC}	Address Access Time	–	120	–	150	
t_{CE}	Chip Enable Access Time	–	120	–	150	
t_{CED}	Output Disable Time	–	50	–	50	
t_{OH}	Output Hold Time	5	–	5	–	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Times	5ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	10	

*This parameter is periodically sampled and is not 100% tested.

Timing Waveforms